REMARKS/ARGUMENTS

Prior to this Amendment, claims 1-3, 5, 7, 10, 12, 17-22, and 32 were pending in the application.

It is first noted that the Examiner has withdrawn the previously-stated anticipation rejections based on "Operating Systems, Design and Implementation" ("Tanenbaum") and based on U.S. Pat. Publ. No. 2003/0181205 ("Yiu").

Claim 32 is amended to correct a typographical error.

After entry of the Amendment, claims 1-3, 5, 7, 10, 12, 17-22, and 32 remain for consideration by the Examiner.

Rejections under 35 U.S.C. §112

In the Office Action mailed February 10, 2006, claims 1-3, 5, 7, 10, 12, and 17-22 were rejected under 35 U.S.C. 112, first paragraph as failing to comply with the written description requirement. This rejection is traversed based on the following remarks.

The Office Action indicates that according to "Applicant's arguments various prior art bus bridges/controllers identified in the prior rejections are not capable of conducting mass storage transactions, implying that the claimed bus controller plays an active role in conducting the mass storage transaction rather than just being a conduit that provides access paths for such transactions." The Office Action states that the bus controller is not described as being different or special in its features compared with any other bus/bridge controllers. The arguments provided in the prior Amendment state that Tanenbaum "fails to show a bus controller associated with its CPU that can 'conduct mass storage transactions' as called for in claim 1."

Applicant was simply trying to stress that "the Disk controller with DMA" cited at page 3 of Tanenbaum does not perform each and every function called for in claim 1, such as conducting mass storage transactions, or include all the limitations stated in claim 1 for the bus controller (e.g., where is the bus controller in Tanenbaum that would conduct mass storage transactions?). Applicant was not trying to imply additional

limitations for this element of the claims, to provide a particular construction of "to conduct," or to read limitations into the claim from the specification. Because "operable to conduct mass storage transactions" is supported as required by 35 U.S.C. 112, first paragraph, Applicant requests that this rejection be withdrawn.

Also, claim 32 was rejected as being indefinite because "process" had no antecedent basis. This word has been changed to "processor."

Rejections under 35 U.S.C. §102

In the February 10, 2006 Office Action, the rejection of claims 1-3, 5, and 21 under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. Publ. No. 2003/0037198 ("Hunsaker") was maintained. This rejection is traversed based on the following remarks.

As amended, claim 1 calls for a bus controller having a memory interface to data memory and to a mass storage interface "without an intermediary mass storage controller." The claimed system provides a significant improvement over prior art systems, such as that shown in Figure 1 of Applicant's specification, because of the removal of the mass storage controller 103 and its additional interfaces and other complexities. Such an improvement is shown by way of example in the system of Figure 2, which shows a bus controller with an interface to both data memory and to a mass storage interface without a mass storage controller.

As discussed in the prior Amendments, Hunsaker shows a system in which the mass storage devices couple to the processor through 2 intermediate mechanisms, the MCH 130 and the ICH 150. Claim 1 calls for the "bus controller" to have "a memory interface coupled to the data memory and a mass storage device's interface without an intermediary mass storage controller." Neither the memory controller hub 130 or the ICH 150 has both an interface coupled to the data memory and a mass storage interface. The Office Action appears to be combining the two controller hubs (MCH 130 and ICH 150) into a single controller as the Office Action states that the ICH 150 is coupled to system memory 140 via MCH 130 and to mass storage device directly, which the Examiner feels meets the limitations of the bus controller of claim 1.

Applicant disagrees with this construction of the claim language of claim 1 and the teaching of Hunsaker. It is not proper to treat the combination of MCH 130 and ICH 150 as a single device as it is core to the Hunsaker device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claim 1 eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Hunsaker. Specifically, claim 1 requires that the bus controller has a memory interface "coupled to the date memory" and this is not taught by a connection via another controller (i.e., via MCH 130). Instead, Hunsaker would lead one skilled in the art to provide interfaces between the controllers 130 and 150 as is the case between the prior art controllers 101 and 103 shown in Applicant's Figure 1. Further, the MCH 130 would have the memory interface that is coupled to the system memory 140 not the ICH 150. But, if the MCH 130 also cannot be the bus controller of claim 1 because it does not have a mass storage interface coupled to the mass storage device's interface.

The Response to Arguments on page 12 of the Office Action disagrees with the above argument. The Examiner states that the "ICH also directly interfaces with the memory hub controller 130, which is a memory interface." Then, the Examiner goes on to state that "Applicant has not shown why an interface to a memory controller is not a memory interface." Claim 1 calls for the bus controller to have "a memory interface coupled to the data memory." The Examiner states that ICH 130 directly interfaces with memory controller hub (MCH) 150 in Hunsaker's Figure 1. However, as discussed above, this is a controller to controller interface and does not teach an interface on the ICH 150 to system memory 140. All the interfacing functionality with system memory 140 is provided by MCH 150 and not by the interfaces between controllers 130 and 150. A person skilled in the art would be unlikely to construe an interface between controllers 130 and 150 to be a "memory interface coupled to the data memory" as called for in claim 1.

Further, from a review of paragraphs [0019] and [0020], it seems that the ICH 150 is more similar to the prior art bus controller 101 shown in Applicant's Figure 1 than

the bus controller of claim 1 (such as controller 201 of Applicant's Figure 2). Specifically, the ICH 150 is described as including a PCI bus interface and USB interfaces (as is the case with controller 101) that would enable it to interface with interfaces of a mass storage controller, such as controller 103 of Applicant's Figure 1. There is no description in these paragraphs regarding ICH 150 that there is no mass storage controller provided in mass storage device 170 or that the ICH 150 is configured to "conduct mass storage transactions between the data memory and the mass storage device."

The Response to Arguments indicates that the Examiner did not find this argument persuasive because the "absence of discussion of there being no mass storage controller does not imply its presence." While this line of reasoning may hold some weight, the absence of a discussion in Hunsaker regarding "a mass storage interface coupled to the mass storage device's interface" does imply that the controller or ICH 150 communicates with the mass storage device 170 in a standard manner. Otherwise, Hunsaker would have provided a discussion of an interface similar to the one described by Applicant. Because no discussion of the "mass storage interface" called for in claim 1 is provided in Hunsaker for the ICH 150, this reference does not teach or suggest such a direct interface (e.g., the only teaching of such an interface is Applicant's own specification and without such teaching a person reading Hunsaker would likely assume an interface more like that shown in Applicant's Figure 1). The Response to Arguments does not rebut Applicant's argument that the ICH 150 fails to include a mass storage interface coupled to the mass storage device's interface. For these reasons, Hunsaker fails to teach the bus controller of claim 1 and does not anticipate the system of claim 1. Claims 2, 3, 5, and 21 depend from claim 1 and are believed allowable at least for the reasons provided for allowing claim 1 over Hunsaker.

Also, the Office Action maintained the rejection of claims 1, 12, and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,601,126 ("Zaidi"). This rejection is traversed based on the following remarks.

As discussed in prior responses, in Fig. 28, Zaidi shows a computer architecture in which a bridge device, not a data/control bus, couples various components. Hence,

there is no controller coupled to the CPU bus as called for in claim 1, nor is there a data memory coupled to the processor as called for in claim 1. Instead, the DRAM is coupled to the memory bus (m-bus). Moreover, Zaidi does not teach that the bridge is capable of conducting mass storage transactions between the data memory and the mass storage device. Similarly, Zaidi does not teach that the MAC is capable of conduct mass storage transactions between the data memory and the mass storage device. For these reasons, claim 1 is not anticipated by Zaidi. Claims 12 and 20, which depend from claim 1, are allowable over Zaidi for at least the same reasons as claim 1.

In the Response to Arguments, the Examiner states that the above discussion does not provide any evidence or well-reasoned logical arguments that certain limitations are not taught. Applicant disagrees as the above statements provide references to specific component cited by the Examiner in the rejection of the claims and explains why these fail to shown the bus controller element of claim 1. Specifically, the arguments provided are well-reasoned in that the Examiner has failed to make a prima facie case of anticipation because each and every element of the claim is not shown by Zaidi because the combination of the bridge and MAC do not meet the limitations of claim 1 for the bus controller (e.g., do not show a controller and do not show a controller that operates to conduct mass storage transactions between the data memory and mass storage). Further, the above arguments explain in detail how Zaidi fails to show data memory coupled to a processor. Hence, Applicant believes the he has fully complied with the requirements of 37 C.F.R. 1.111(b) and requests that these arguments be rebutted by the Examiner or the rejection withdrawn.

Further, the Office Action maintained the rejection of claims 1, 14, and 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Pat. No. 6,128,669 ("Moriarty"). This rejection is traversed based on the following remarks.

The Office Action cites Moriarty as teaching all the limitations of claim 1 in its Figure 1. However, in Figure 1, Moriarty shows a computer architecture in which a bridge device 106 is required for mass storage transactions. Hence, Moriarty does not show a bus controller that includes both a mass storage interface and an interface to the data memory as called for in claim 1. Instead, memory controller 108 enables

memory transactions between the processor and the memory and a separate bridge 106 enables mass storage transactions. Hence, mass storage transactions must traverse multiple interfaces including the SCSI controller, PCI Bus, and Host bus. This multiple bus traversal is minimized in the invention of claim 1. Specifically, claim 1 calls for the bus controller to include a memory interface coupled to the data memory, which is not shown as discussed above in Moriarty, and claim 1 calls for the bus controller to also include a mass storage interface coupled to the mass storage device's interface, which is not, as is discussed above, shown by element 106 and 120 of Moriarty. Claims 14 and 20, which depend from claim 1, are allowable over Moriarty for at least the same reasons as claim 1.

The Response to Arguments again attempts to rebut these arguments by stating that they are not evidence or are not well-reasoned. Applicant disagrees because he has shown that the two interfaces required to be in the bus controller of claim 1 are not shown by Moriarty. The Response to Arguments also states that there is nothing in the claim elements that "precludes multiple bus traversals." However, the claims do call for the two interfaces of the bus controller are coupled to the data memory and to the mass storage device's interface which precludes traversal of the number of interfaces that would be required in the Moriarty system. Hence, Applicant has met his burden of specifically mapping the claim limitations to the deficiencies of Moriarty and its failure to anticipate or suggest at least the bus controller of claim 1.

Still further, the Office Action maintained the rejection of claims 1 and 19 under 35 U.S.C. §102(e) based upon U.S. Pat. Appl. Publ. No. 2002/0144121 ("Ellison"). This rejection is respectfully traversed as claim 1 is believed allowable over Ellison at least for the reasons provided for allowing claim 1 over Hunsaker because Ellison's Fig. 1C and Hunsaker's Figure 1 provide similar teaching, and hence, have similar failings relative to claim 1.

Further, as discussed in prior amendments, Ellison shows a system in which the mass storage devices couple to the processor through an intermediate mechanism, the ICH 150. Neither the memory controller hub 130 or the ICH 150 have both an interface coupled to the data memory and a mass storage interface. It is not proper to treat the

combination of MCH 130 and ICH 150 as a single device as it is core to the Ellison device that these elements be implemented as separate devices. As such, they introduce a mandatory interface between the devices that must be traversed by mass storage transactions. The invention of claims 1 and 19 call for a single controller having a memory interface and a mass storage interface that eliminates this need for excessive interface traversal and therefore provides an improvement over the architecture of Ellison.

Further, the same Response to Arguments were applied to Applicant's arguments regarding Ellison as were provided for Hunsaker. As a result, the discussion provided regarding the Response to Arguments and the reasons for allowing claim 1 over Hunsaker are believed equally applicable to the use of Ellison in rejecting claim 1. Specifically, the Examiner seems to be asking to have it both ways by arguing that the ICH 150 could have both interfaces called for in claim 1 although they are not shown or discussed in Ellison but the mass storage devices do not have an intermediary mass storage controller because none is shown (e.g., if Examiner is correct that the failure to discuss a mass storage controller means there is not one, then that is also true at least for the memory interface of the bus controller of claim 1 as a claimed element cannot just be presumed to exist in a reference even though no coupling between the ICH 150 and the system memory is shown).

Additionally, claims 17 and 18, which depend from claim 1, were rejected under 35 U.S.C. §102(e) based upon U.S. Pat. No. 6,493,656 ("Houston"). This rejection is respectfully traversed because the bus controller of claim 1 is not shown by the controller 102 of Houston or by the combinations of 102 and 114 or 102 and 121. Claim 1 calls for the bus controller to interface with a mass storage device without a mass storage controller as would be the case with HDs of Houston, e.g., see Figure 2, controller 214. Again, the only rebuttal of these arguments in the Response to Arguments was that arguments were not well-reasoned, but the arguments discuss the specifically-cited components of Houston and explain how these do not teach the bus controller of claim 1 and its two specific interfaces and their coupling. Hence, Applicant has provided arguments that if fully considered should overcome the rejections.

Further, as discussed in the prior amendments, Houston shows a computer architecture that lacks a controller having a memory interface and a mass storage interface. North Bridge element 102, by itself, has only a memory interface and a PCI bus interface, not a mass storage interface. Accordingly, Houston does not show or fairly suggest the invention of claims 17 and 18 because it fails to show at least the bus controller of claim 1.

Rejections under 35 U.S.C. §103

In the February 10, 2006 Office Action, the Examiner provided new claim rejections. The Office Action rejects claims 7, 10, and 32 under 35 U.S.C. §103(a) as being unpatentable over Hunsaker, Zaidi, Moriarty, or Houston in view of Tanenbaum. This rejection is traversed based on the following remarks.

Claims 7 and 10 depend from claim 1 and are believed allowable over Hunsaker, Zaidi, Moriarty, or Houston when considered alone for the reasons provided above for allowing claim 1 over each of these references. The addition of Tanenbaum to the teachings of these references does not make claims 7 and 10 obvious because Tanenbaum fails to overcome the deficiencies of the base references with regard to claim 1. Significantly, Tanenbaum had previously been cited by the Examiner as anticipating claim 1, but those rejections have been withdrawn presumably because the reference did not show all the limitations of claim 1 (or suggest each limitation as Tanenbaum is not being cited by itself as making the system of claim 1 obvious). Hence, Applicant requests that the rejection of claims 7 and 10 based on Hunsaker, Zaidi, Moriarty, or Houston in view of Tanenbaum be withdrawn.

More particularly, Tanenbaum fails to teach each and every limitation of claim 1 (or to at least teach the missing bus controller of claim 1). Tanenbaum does not teach the bus controller of claim 1 with its "Disk controller with DMA." This disk controller is a mass storage controller as shown in Applicant's Figure 1, and Tanenbaum fails to show a bus controller associated with its CPU that conducts mass storage transactions as called for in claim 1. Tanenbaum, therefore, does not overcome the base references' deficiencies because at least the bus controller configured as required by the language of claim 1 is not shown or even suggested by Tanenbaum.

Further as discussed in the prior Amendment, claim 1 calls for a data memory coupled to and shared by both the processor and the mass storage device. The disk controller in Tanenbaum is not a mass storage device as called for in claim 1 but is instead an interface to a mass storage device labeled "disk" in Tanenbaum, i.e., is a mass storage controller with such an interface. However, even if the disk controller were to be integrated with the disk in Tanenbaum, the reference shows a disk controller having memory (labeled "buffers") that is separate from and independent of the block labeled memory. Tanenbaum does not fairly suggest that the disk controller buffers could be implemented in the memory, or that the memory could be implemented by the disk controller buffers, so as to provide a data memory coupled to and shared by both the processor and the mass storage device as called for in claim 1. For these additional reasons, claim 1 is allowable over the Tanenbaum reference when considered alone or in combination with the other four references. No rebuttal of this description of Tanenbaum was provided in the Office Action in the Response to Arguments.

Independent claim 32 is directed to a system with some limitations similar to that of claim 1, and as a result, the reasons for allowing claim 1 over the four base references and Tanenbaum are believed applicable to claim 32. Further, claim 32 calls for a first mass storage device with an interface and the first mass storage device is coupled to a data/control bus. A processor is coupled to this same bus and implements mass storage control processes to control the first mass storage device. A second mass storage device with an interface is provided along with a bus controller that has a mass storage interface coupled to the second mass storage device's interface. Data memory is provided that is coupled to the data/control bus and the bus controller conducts mass storage transactions between the data memory and the second mass storage device.

As can be seen, there are similarities between the system of claim 1 and claim 32, but the system of claims 32 calls for additional components and a specific arrangement not required in claim 1. Hence, a prima facie case of obviousness has not yet been stated for claim 32 by the Office as the rejections of claim 1 based on Hunsaker, Zaidi, Moriarty, and Houston are directly applied to claim 32 without

accounting for the different or additional components and their interfaces/couplings. Applicant requests that the rejection of claim 32 be withdrawn or a proper case of obviousness be made with a showing of where each element in the claim is shown or suggested (e.g., the Office must show two mass storage devices, a data/control bus, a processor implement mass storage processes, and the bus controller as claimed in claim 32).

Yet further, claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hunsaker in view of U.S. Pat. Publ, No. 2003/0181205 ("Yiu"). This rejection is respectfully traversed because claim 22 depends from claim 1 and Yiu fails to overcome the deficiencies of Hunsaker pointed out above with reference to claim 1. As with Tanenbaum, Yiu was previously cited as an anticipatory reference, but rejections based on Yiu with regard to claim 1 were withdrawn.

Specifically, Yiu in Figure 3 and elsewhere fails to show the bus controller of claim 1 that is provided for interfacing with mass storage devices without a mass storage controller. In Paragraph [0034] the processor 31 is described as having some similar features as the bus controller of prior art system in Applicant's Figure 1 for interfacing with a mass storage controller of the storage 34 of Yiu. Hence, the bus controller that interfaces with a mass storage device without an intermediary mass storage controller is not shown or suggested by Yiu.

Further, as discussed in the prior amendments, the Examiner relies on Fig. 3 of Yiu et al. to show the specific architecture called for in claim 1. However, Yiu states in paragraph 32 that "...FIG. 3 is not intended to represent any one specific physical arrangement." Accordingly, Fig. 3 does not show a real computer architecture and cannot be relied on to show or suggest the limitations of claims 1, 13-6, and 20-22. Specifically, one cannot, even today, obtain a mass storage device 34 such as a magnetic disk or CDROM that interfaces directly to the same bus as RAM and a processor. Yiu does not identify any such devices and so fails to provide an enabling disclosure of such a system. In contrast, the present invention teaches how to build such a system including such a mass storage device by providing a controller having a memory interface and a mass storage interface. The list of various devices that

appears in paragraph 34 of Yiu et al. describe types of processors and does not disclose a single device that would show or suggest the controller of claim 1. Claim 22 that depends from claim 1 is distinct over Yiu for at least the same reasons as claim 1. Note, no rebuttal of this lack of teaching by Yiu with regard to claim 1 was provided in the Response to Arguments.

Conclusion

In view of all of the above, it is requested that a timely Notice of Allowance be issued in this case.

No fee is believed due with this Amendment. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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